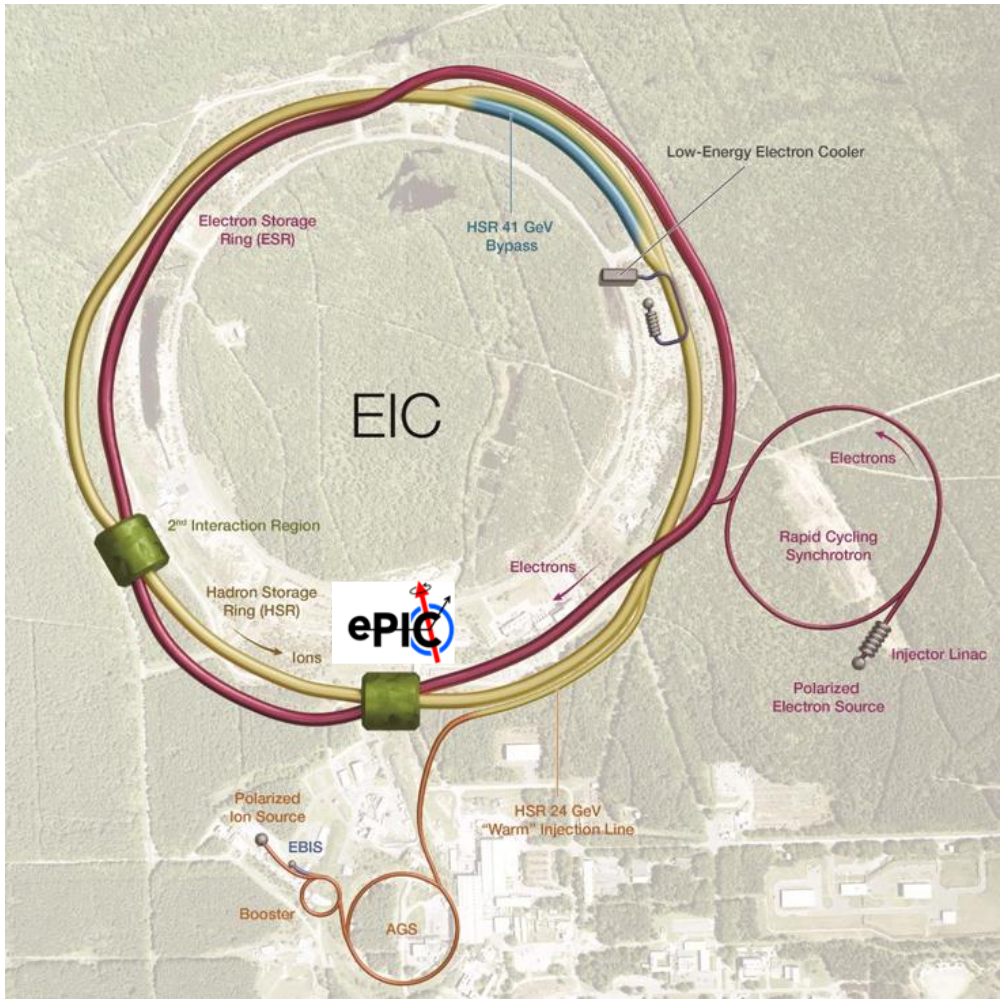
The readout of the forward dual RICH at ePIC: irradiation tests of key electronic components



2nd European Summer School for the Physics of the EIC and Related Topics

Author: Sandro Geminiani
(University and INFN of Bologna)

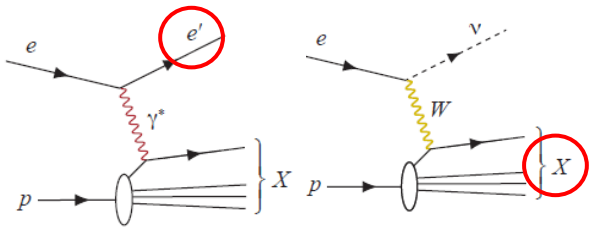
Date: 30/06/2025

The role of PID in EIC physics

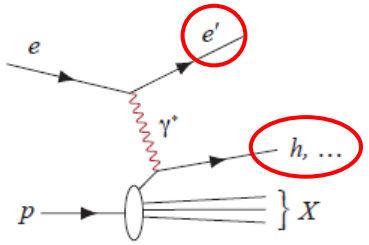
The future **Electron Ion Collider** provides **e+p/Ion collisions**:

- $20 < \sqrt{s} < 140$ Gev
- $L_{e+p} = 10^{33} - 10^{34}\ cm^{-2}s^{-1}$.
- Highly polarized electron and proton beams (~70%).
- **Physics purpose**: studying the **internal structure of nucleon**, **nucleon properties** (mass, spin ecc…), **QCD processes in a nuclear medium** and **much more**..

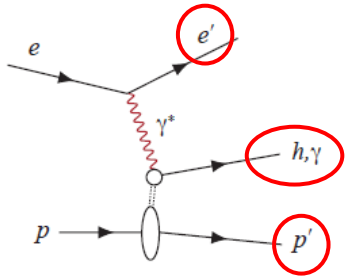
DIS



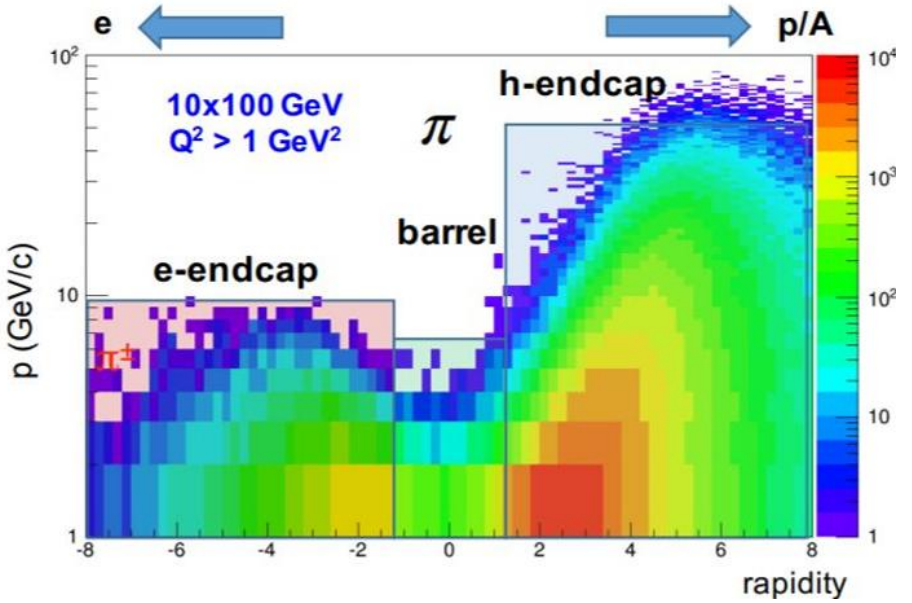
SIDIS



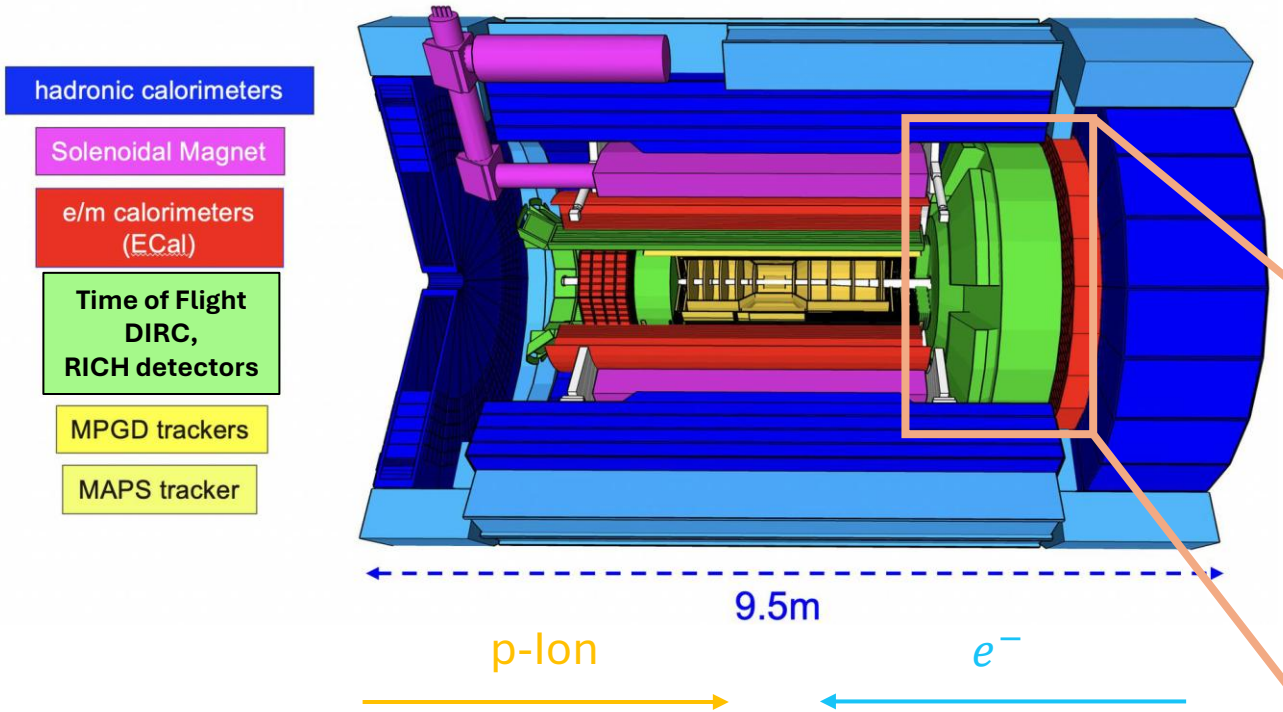
Exclusive DIS



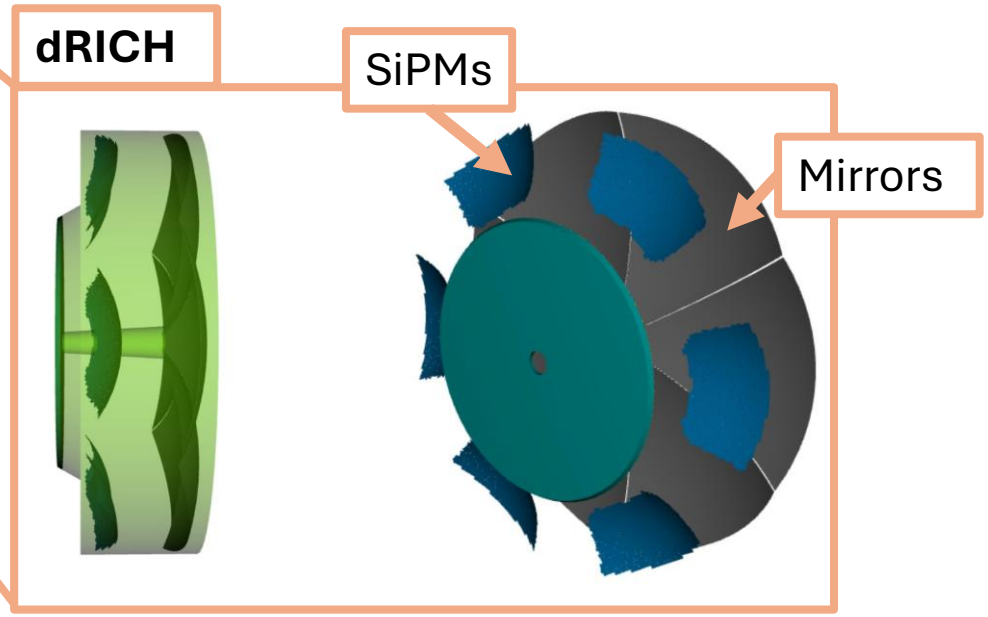
Different channels will be inspected and a **PID** covering a **wide phase-space** is needed, as shown in the plot below:



The ePIC experiment and the dRICH



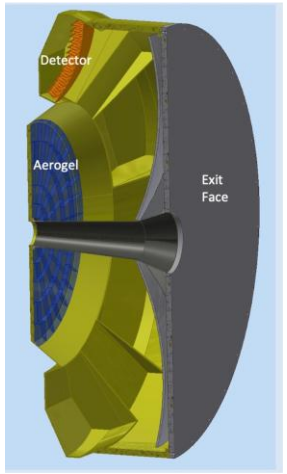
- **Compact detector in η** = [1.5-3.5]
- **~1 T** magnegtic field
- **π/K/p separation** in 3-50 GeV/c range
- **e-identification** up to 15 GeV/c
- **Streaming readout system**



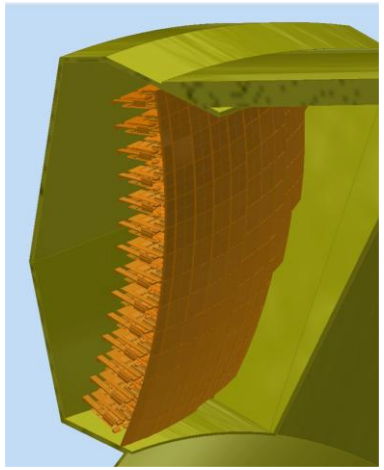
- **RICH with 2 Cherenkov radiators** (aerogel and C_2F_6 gas)
- More than **300000 SiPMs**

The dRICH readout system

dRICH section



Detector box



The **dRICH sector** design includes 208 **Photon Detection Units.**
(1248 PDUs in the dRICH)

Each **PDU** is a compact system reading and controlling up to **256 SiPMs.** A **10 Gb/s downlink** up to the I-DAM level is used.

Ref:
https://agenda.infn.it/event/43344/sessions/31801/#20250121

[14-1400] Gb/s

DAM level

300 Gb/s

Up to **42 PDU links** to the **FELIX-155** board are needed (100 Gb/s downlink each).

I-DAM level: 30 FELIX-155, working both as **concentrator** and for **data reduction**
(NN processes + physics tagger).

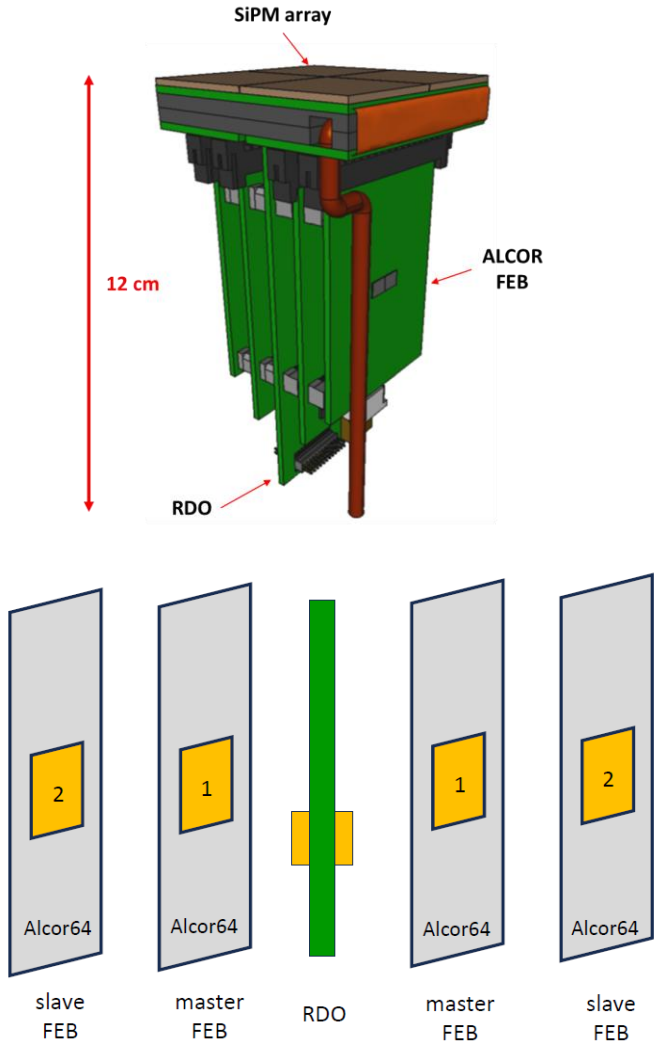
ePIC processing and storage system

All **30 FELIX** links are aggregated providing a limit bandwidth of **300 Gb/s**.

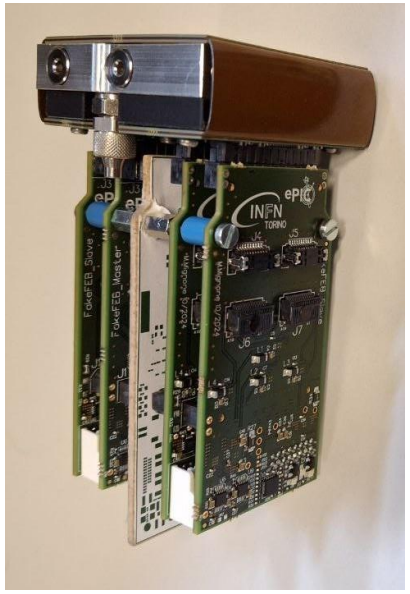
A **clock synchronous** with the bunch crossing frequency (**98.5 MHz**) is distributed to the ePIC-DAQ.

The PDU layout

PDU scheme



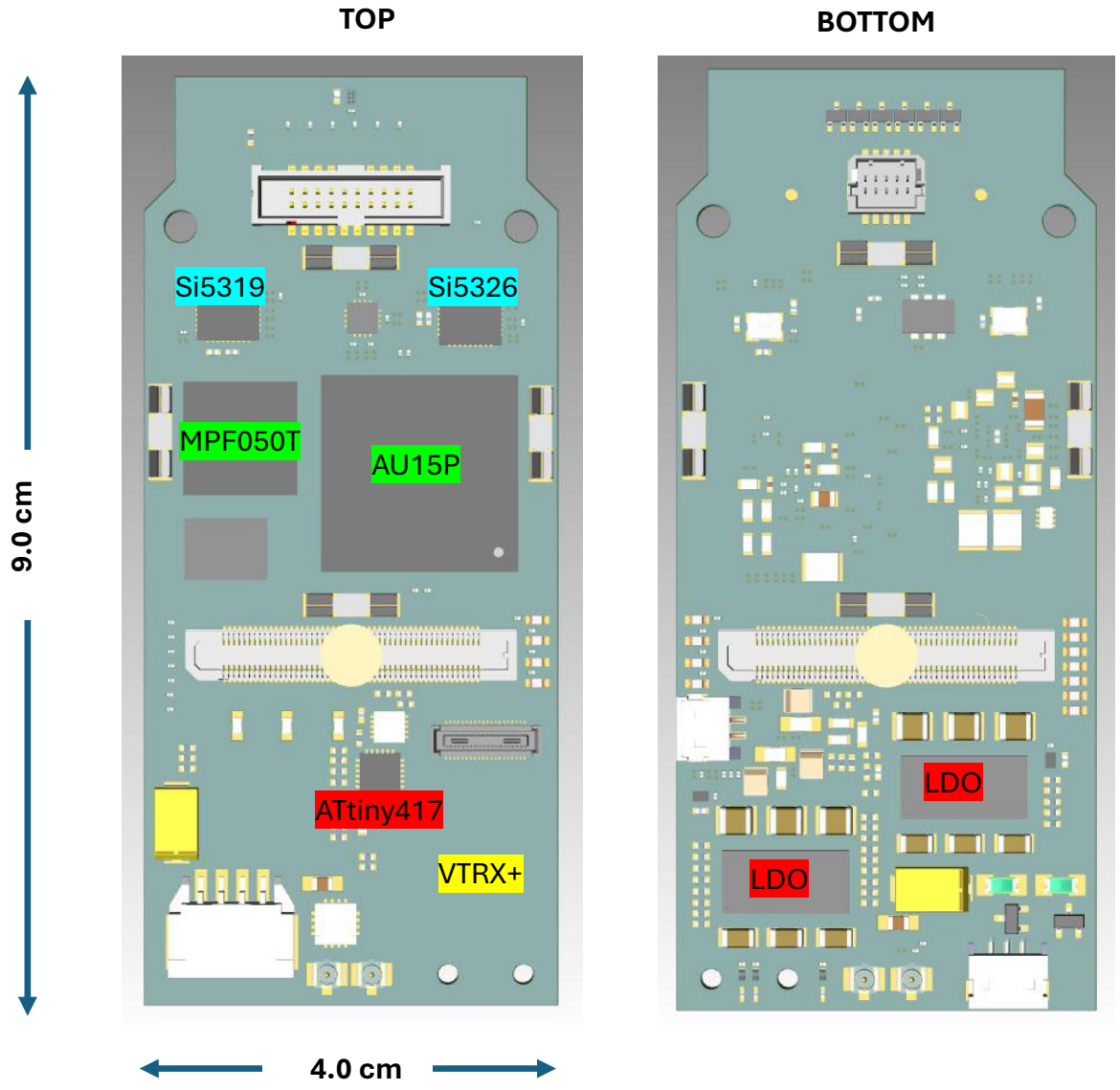
PDU pre mock-up



The PDU layout includes 5 custom boards, which host different components:

- **ALCOR FEB**: it hosts the **ALCOR64** ASIC, designed to digitize the timing data, coming from **64 SiPMs**, using a **394 MHz** clock frequency and analog interpolation TDCs.
- **RDO card:** it is an **FPGA-based card** hosting two different FPGAs for the **configuration** and **readout** of 4 ALCORs. The board has been designed to provide:
  1. **A small and compact layout like the FEBs**
  2. **A 10 Gb/s optical fiber link**
  3. **Low jitter clock distribution to ALCORs (very high speed frequency signals inside the FPGAs).**
  4. **High reliability**

The RDO card



Ref: https://indico.bnl.gov/event/26445/

FPGAs

- **AU15P**: **AMD Artix Ultrascale+** main FPGA interfacing with ALCORs.
- **MPF050T**: **Microchip PolarFire** FPGA responsible for the AU15P configuration (**see later …**).

Clock multiplier

- **Si5319** and **Si5326** from **Skyworks Solutions**.

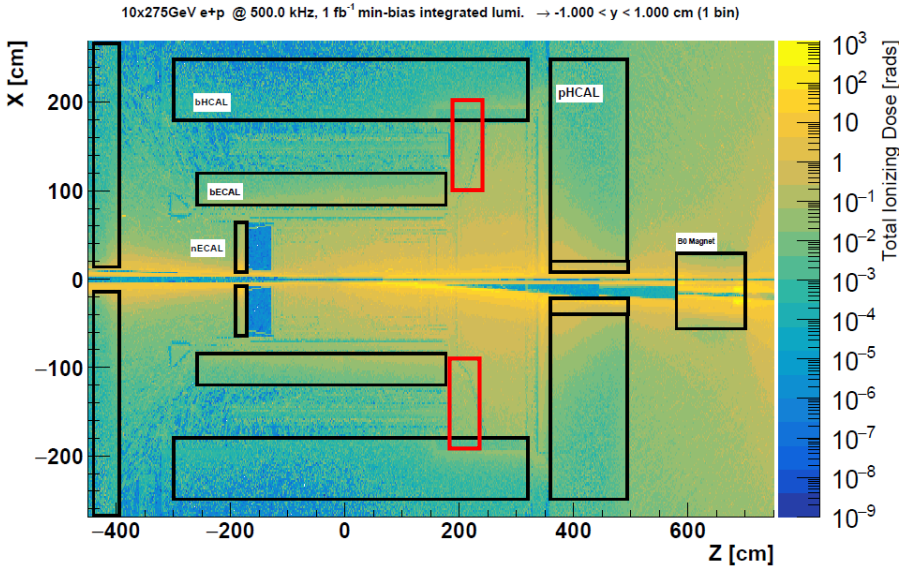
Power management

- **2 LDOs LTM4709** for different power rails.
- **Microchip ATtiny417** µcontroller, controlling power consumption.

Data link

- **VTRX+**: optical transceiver (not plugged in the picture)

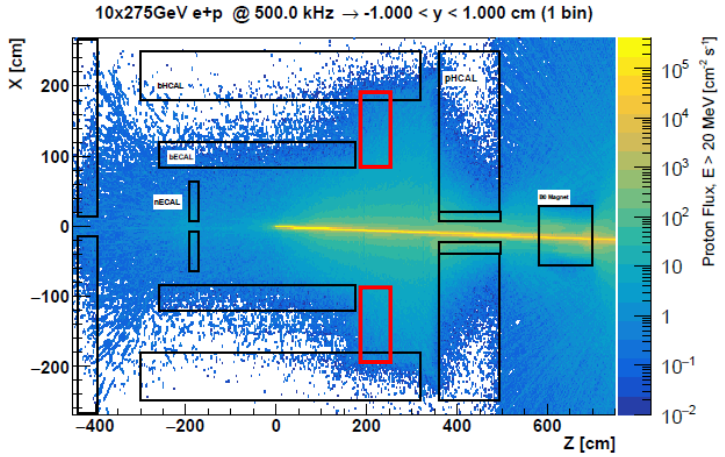
The PDU radiation environment

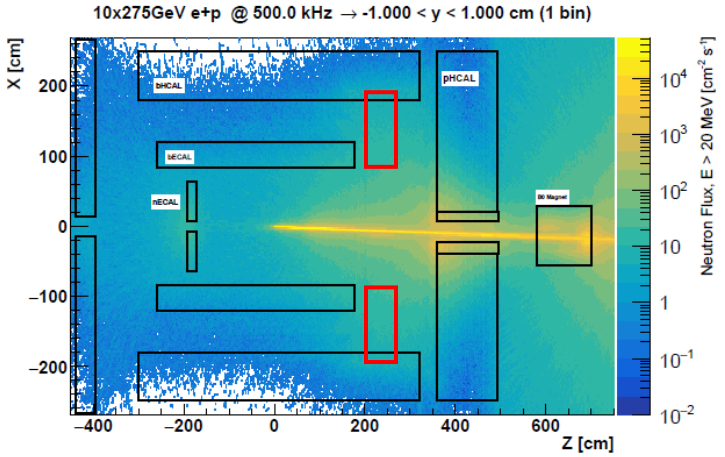


The dRICH-PDUs are in a moderately hostile radiation environment.
Expected radiation exposure, including a 5 safety factor:

$$\mathrm{TID}_5 \cong 2.3\ \mathrm{krad}\ (\text{for } 1000\ \mathrm{fb}^{-1})$$

$$\phi_5(\mathrm{p}+\mathrm{n} > 20\mathrm{MeV}) \cong 700\ \mathrm{Hz/cm}^2$$



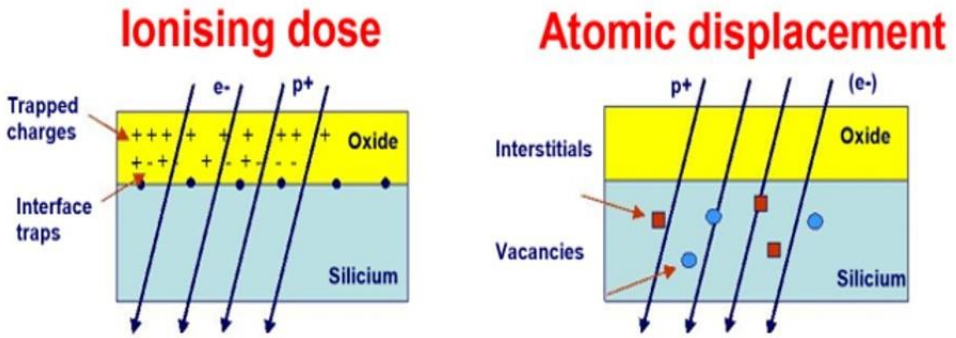


This environment leads to important issues for the dRICH detector as:

- SiPM degradation
- **Need to check electronics stability vs effects of radiation**

Radiation effects on electronics

Cumulative effects



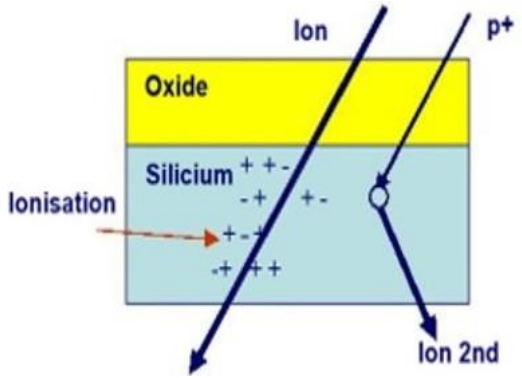
During component life a cumulative radiation quantity affects the device performance:

- **Ionizing effect**: **TID** generates bulk traps and SiO_2 surface traps, modifying the V_t of the silicon material.
- **Non-ionizing effect**: displacement of a lattice atom in the bulk that modifies the device specifics.

Monitor the device failures over TID = Fluence · $TID_{Si}^{Fluence}$ (E) !

$TID_{Si}^{Fluence}$ **(E) is the estimated TID on a Si device per Fluence unit**

Single Event Effects (SEEs)



A single particle can produce enough ionization to raise the current inside the device:

- **SEU**: a current spike in a silicon cell can produce a signal level inversion, as a bit-flip in a memory cell. **Estimate:**

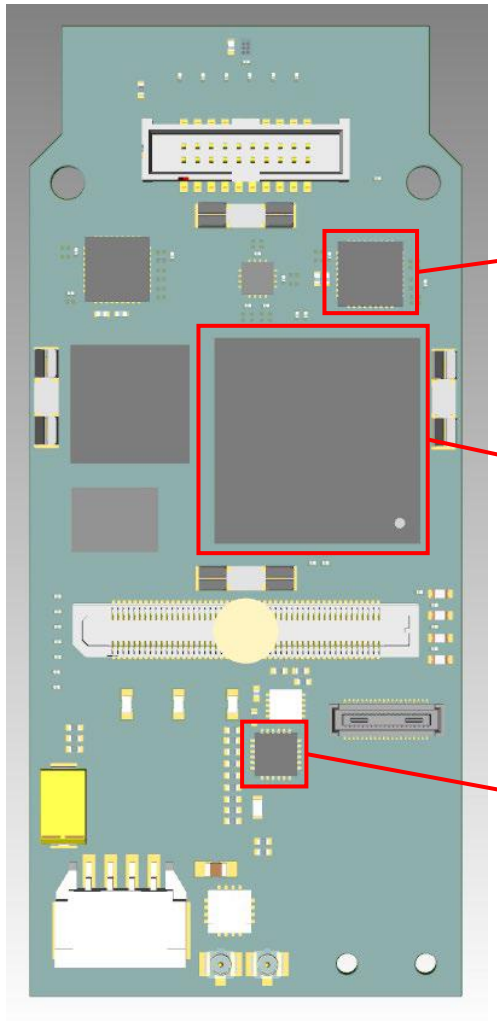
$$1.\quad \sigma_{SEU} = \frac{N_{SEU}}{Fluence \cdot N_{bit}}$$
$$2.\quad MTBF = (\sigma_{SEU} \cdot N_{bit} \cdot Flux)^{-1}$$

- **SEL**: a short circuit inside a silicon cell is generated, raising the current up to a permanent damage.

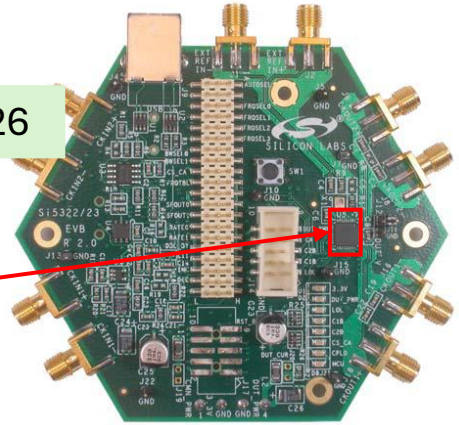
Monitor the current for SEL occurence!

Proton Irradiation campaign at Trento (December 2024)

Ref:
https://agenda.infn.it/event/43344

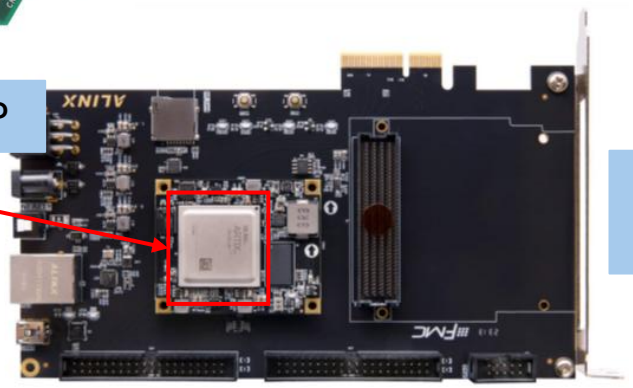


Si5326



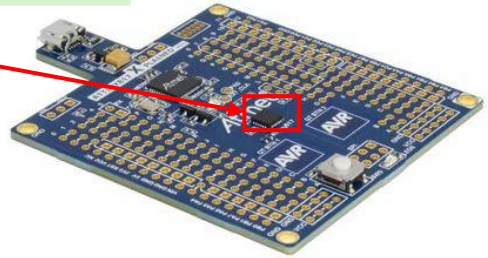
proton beam @ 100 MeV
(flux = 10^8 Hz/cm^2)

AU15P



proton beam @ 70 MeV
(flux = 10^6-10^7 Hz/cm^2)

ATtiny817



proton beam @ 100 MeV
(flux = 10^8 Hz/cm^2)

Si5326 and ATtiny817 setup

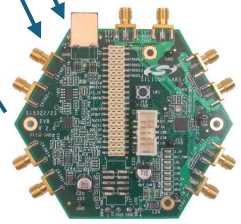
jitter measurement

LV (power and SELs)

Configuration and SEU detection

Clk out at 394 MHz

Clk in



DUT

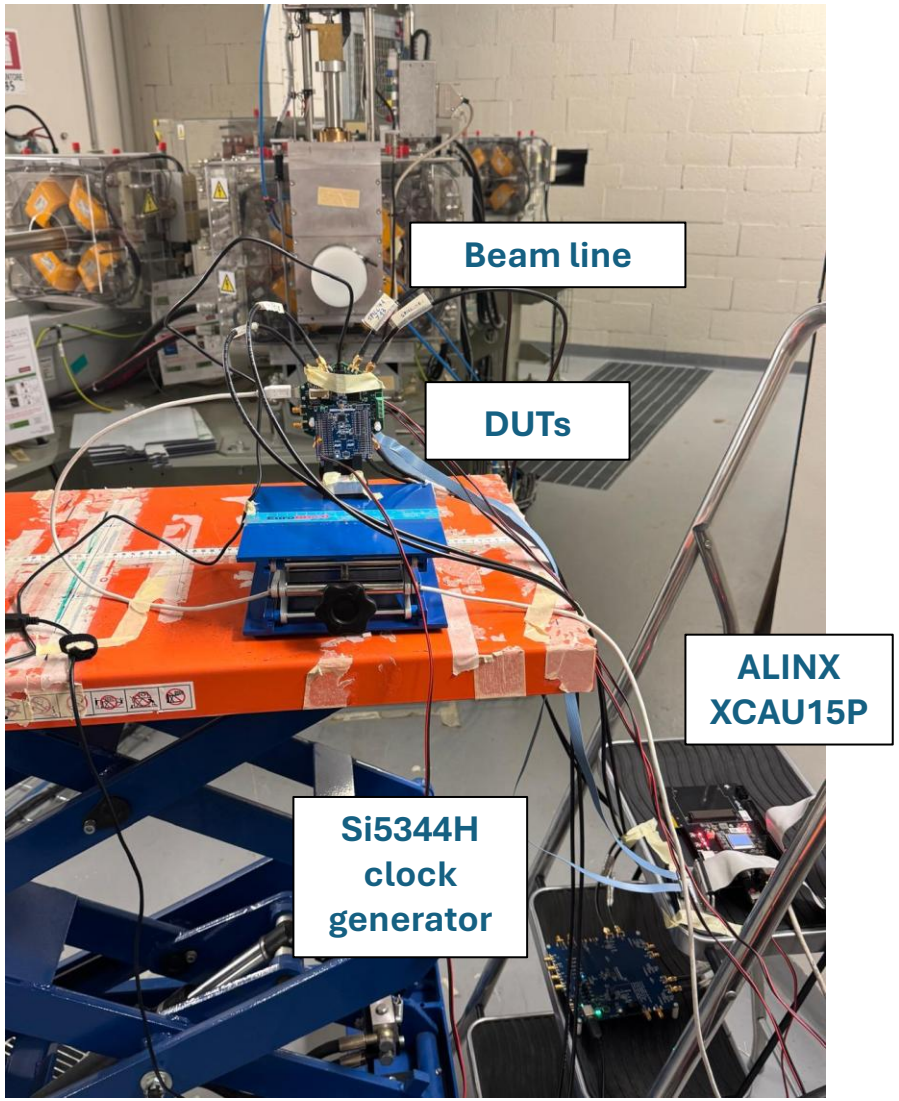
proton beam @ 100 MeV (flux = 10^8 Hz/cm^2)

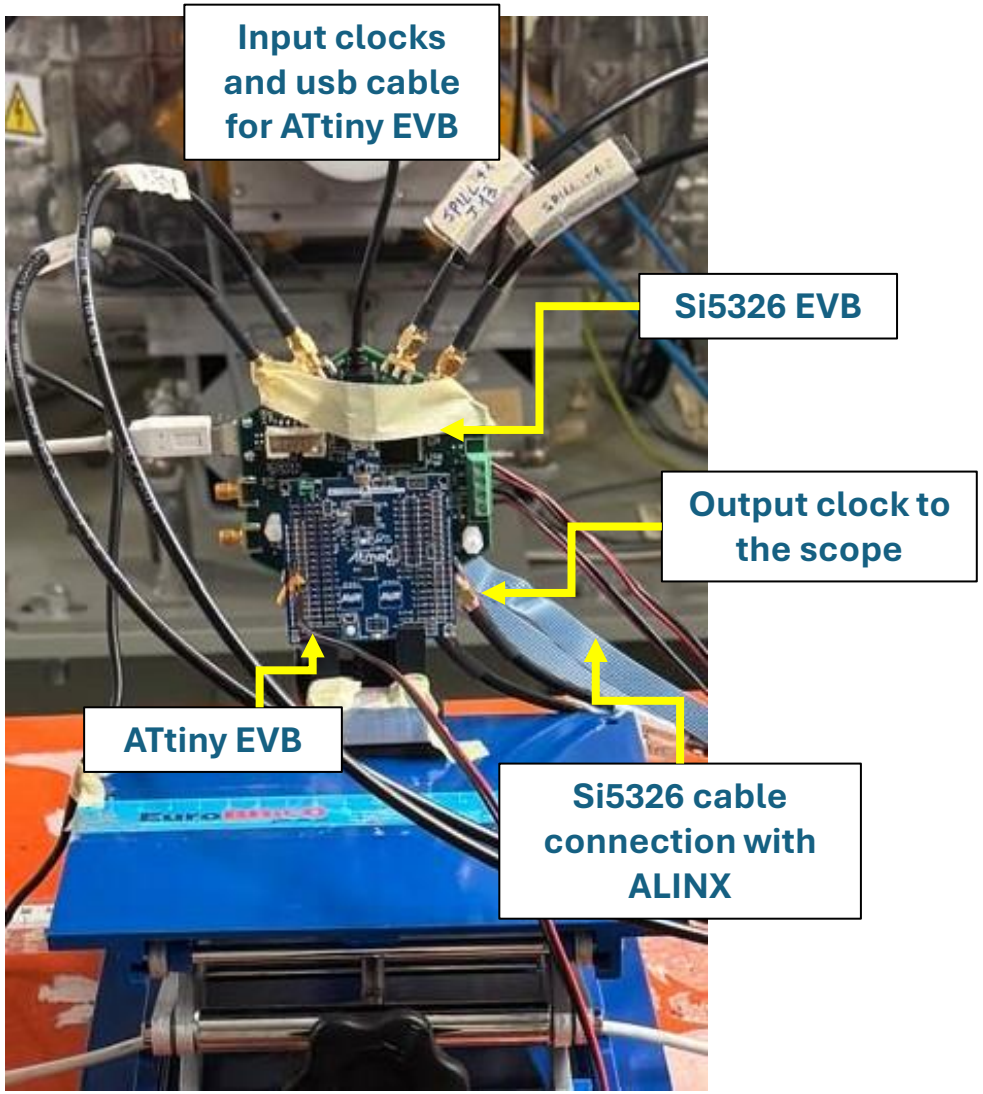
Host PC

Another µC on board is used for UART interface with the ATtiny.

LV (power and SELs)

Si5326 and ATtiny817 setup





Summary of the results

Mean Time Between Failure:
$$MTBF = (\sigma_{SEU} \cdot N_{bit} \cdot Flux)^{-1}$$

Si5326

- **TID = 42 krad** after 1553 s **(dose rate = 1-2 krad/min)**
- **No SEL** detected.
- $\sigma_{SEU} = (2.11 \pm 0.50) \cdot 10^{-14} \frac{\text{cm}^2}{\text{bit}}$
- 394 MHz output **clock was stable during the irradiation**

MTBF in the dRICH system (1248 RDOs) for each Si5319 and Si5326:

3.8 h

ATtiny817 (SRAM = 512 B and FLASH = 8 kB)

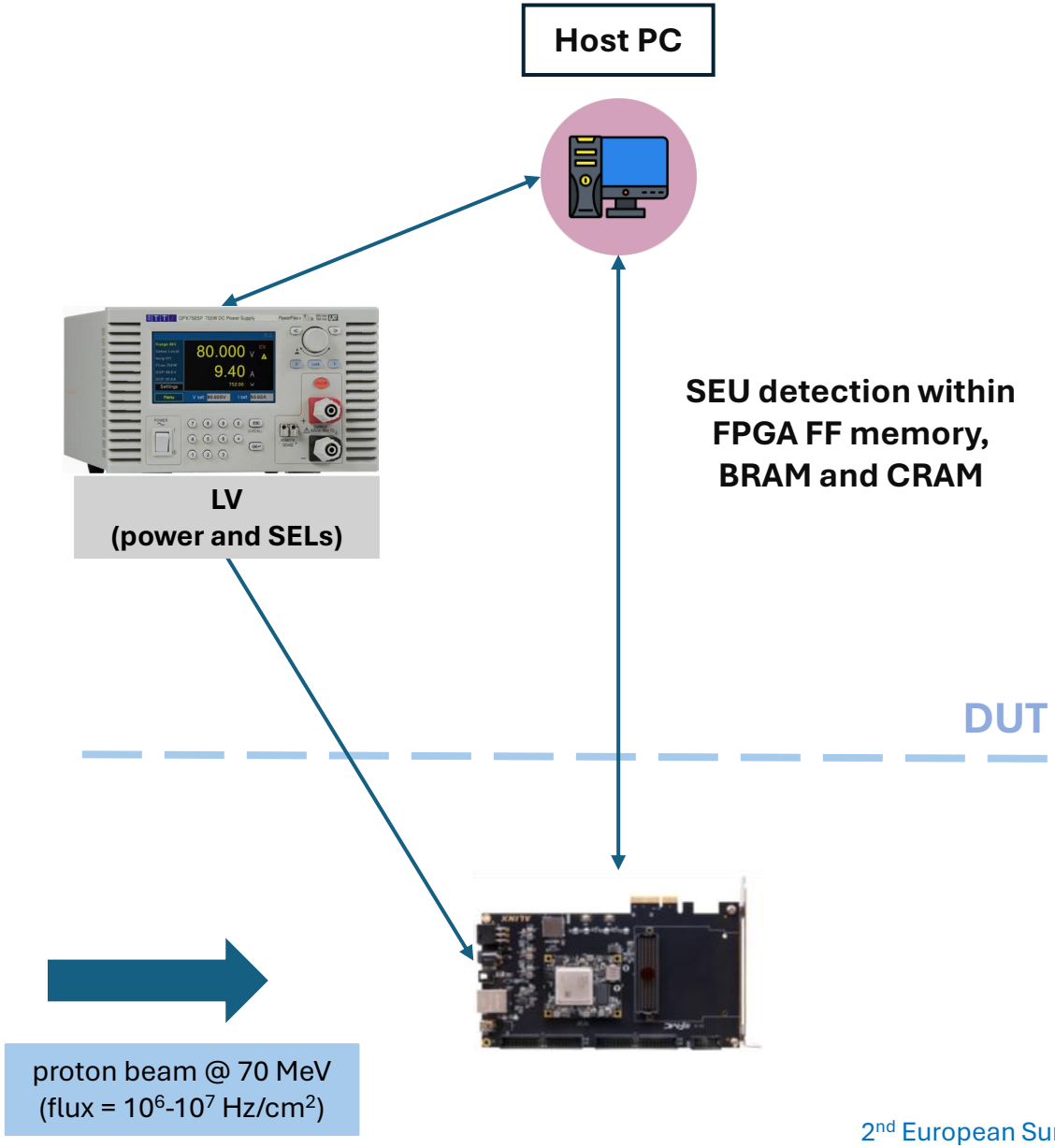
- **TID = 23 krad** after 1026 s **(dose rate = 1-2 krad/min)**
- It **stopped working at TID = 23 krad,** but **no SEL** was detected**.**
- **SRAM**: $\sigma_{SEU} = (3.89 \pm 0.54) \cdot 10^{-14} \frac{\text{cm}^2}{\text{bit}}$
- **FLASH Memory** (limit @ 95% C.L.):

  $\sigma_{SEU} < 2.32 \cdot 10^{-16} \frac{\text{cm}^2}{\text{bit}}$ **(No SEU detected)**

MTBF in the dRICH system (1248 RDOs) for ATtiny417:

SRAM (256B): 4.0 h
FLASH (4kB): > 43 h

ALINX XCAU15P setup



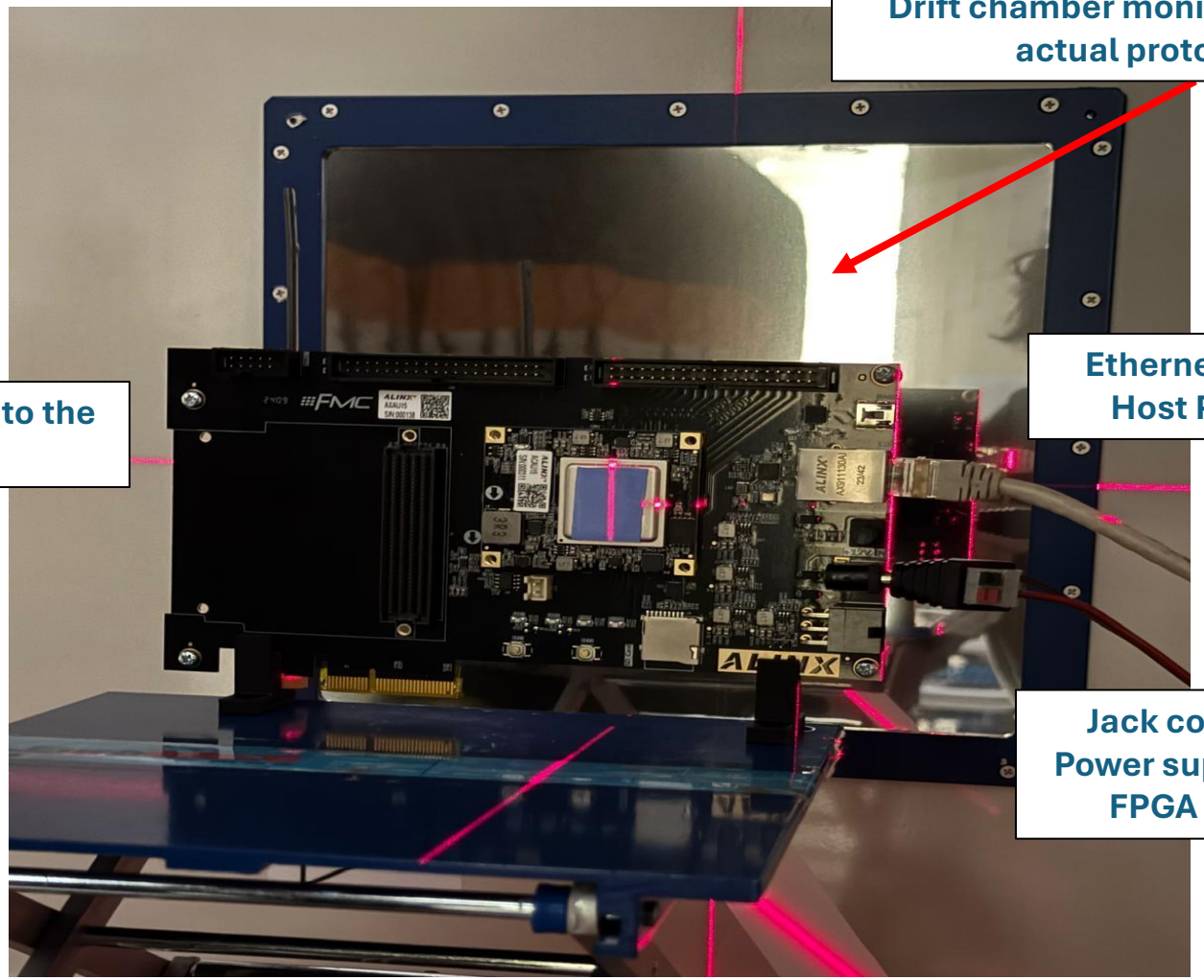
The AU15P checks its own memory (communication via **IPbus over Ethernet link**):

- **FF chains** and **Block RAM buffer** were configured with a **fixed pattern** and checked continuously.
- **Configuration RAM** was checked by the **Soft Error Mitigation (SEM) IP core** by AMD (**ref:** https://www.xilinx.com/products/intellectual-property/sem.html).

The SEM IP is configured in **«mitigation and testing»** mode:

- It **locates the errors** through ECC and CRC approaches.
- It **corrects the error** if the location is identified.
- **It checks all the configuration memory.**

ALINX XCAU15P setup



Drift chamber monitor to measure the actual proton fluence.

ALINX XCAU15P aligned to the beam.

Ethernet Connection to the Host PC to detect SEUs.

Jack connection to the LV Power supply to power up the FPGA and detect SELs.

Summary of the results

AU15P

- **TID = 6.36 krad (dose rate = 10-500 rad/min)** after **3632 s**
- **No SEL** detected after **3632 s**

- **FF Memory** (limit @ 95% C.L.):

$$\sigma_{SEU} < 3.5 \cdot 10^{-14} \frac{\mathrm{cm}^2}{\mathrm{bit}}$$ (**No SEU detected**)

- **BRAM** (it differs for a factor ~2 with the AMD estimate):

$$\sigma_{SEU} = (1.78 \pm 0.23) \cdot 10^{-15} \frac{\mathrm{cm}^2}{\mathrm{bit}}$$

- **CRAM** (it is compatible with the AMD estimate):

$$\sigma_{SEU} = (2.30 \pm 0.28) \cdot 10^{-16} \frac{\mathrm{cm}^2}{\mathrm{bit}}$$

Ref: https://docs.amd.com/r/en-US/ug116/SEU-and-Soft-Error-Rate-Measurements

AMD estimates	$\sigma_{SEU}\left(\frac{\mathrm{cm}^2}{\mathrm{bit}}\right)$
BRAM	$(9.8 \pm 1.8) \cdot 10^{-16}$
CRAM	$(2.67 \pm 0.48) \cdot 10^{-16}$

MTBF in the dRICH system (1248 RDOs): > 3.6 min

MTBF in the dRICH system (1248 RDOs): 2.1 min

MTBF in the dRICH system (1248 RDOs): 2.5 min

Conclusions and outlooks

1. All the Devices were tested up **to a TID largely exceeding expected TID @dRICH: no destructive effects seen for $\mathbf{TID} \leq \mathbf{TID_5}$.**
2. **No SEL** was detected for all the devices, but the ATtiny stopped working after TID = 23 krad.
3. Considering the found MTBF values:
   - **Clock multipliers**: the RDO AU15P will **configure both the chips every t ≪ 3.8 h**.
   - **ATtiny:** the main SRAM registers will be triplicated to implement **TMR** (Triple Modular Redundancy).
   - **AU15P BRAM and FF:** the SEU will be **managed at the AU15P firmware level** (**reset logic** or **CRC code** to recognize the upset).
   - **AU15P CRAM:** the **MPF050T** will read and **write (correct) the CRAM memory (scrubbing).**

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All tested components were validated for the RDO development, but SEU mitigation strategies are needed as expected!

Next Steps

1. Another test with **5 ATtiny817s is foreseen in September** (also the **LDO devices** will be irradiated).
2. The **prototype firmware for the RDO AU15P** has been developed for **future test beams**.
3. The **RDO** has to be **validated**.
4. The **MPF050T firmware is under development** as SEU mitigation strategies for other components.
5. **A proton irradiation campaign for the RDO card is planned for December 2025!**

Next Steps

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5. **A proton irradiation campaign for the RDO card is planned for December 2025!**

Thank You
for Your attention!

Backup

Results of the first setup

ATtiny817 µcontroller

- **Monitored memory:** 6.6/8 kB of **FLASH (53 kb)** and 450/512 B of **SRAM (3.6 kb).**
- **21 SEUs** detected on **SRAM**, while **0 SEUs** on **FLASH** memory after 1026 s.
- **TID = 23 krad (dose rate = 1-2 krad/min)**
- The **ATtiny stopped working at TID = 23 krad** .
- **SRAM**: $\sigma_{SEU} = (3.89 \pm 0.54) \cdot 10^{-14} \frac{cm^2}{bit}$
- **FLASH memory** (limit @ 95% C.L.): $\sigma_{SEU} < 2.32 \cdot 10^{-16} \frac{cm^2}{bit}$

MTBF in the dRICH system (1248 RDOs) for ATtiny417:

SRAM (256B): 4.0 h
FLASH (4kB): > 43 h

Si5326 clock multiplier

- **Monitored memory: 2007/2048 bits** of configuration memory.
- **19 SEUs** and **0 SELs** detected after 1553 s.
- **TID = 42 krad (dose rate = 1-2 krad/min)**
- Besides the SEUs, the device did not **lose the PLL lock keeping the output clock period stable.**
- $\sigma_{SEU} = (2.11 \pm 0.50) \cdot 10^{-14} \frac{cm^2}{bit}$

MTBF in the dRICH system (1248 RDOs) for each Si5319 and Si5326:

3.8 h

Results of the second setup

- **Monitored memory: 8/156 kb** of **FF memory**, **3.6/5.1 Mb** of **BRAM** and **33/33 Mb** of **CRAM**.
- **0 SEUs** detected on **FF memory** and **69 SEUs** on **BRAM** after 2560s.
- **70 corrected SEUs**, **11 uncorrected SEUs** and **1 dead link** detected on **CRAM** after 2560 s.
- **No SEL** detected after 3632 s.
- **TID = 6.36 krad (dose rate = 10-500 rad/min)** after 3632 s.

FF memory (limit @ 95% C.L.): $\sigma < 3.5 \cdot 10^{-14} \frac{\mathrm{cm}^2}{\mathrm{bit}}$

MTBF (156 kb) in the dRICH system (1248 RDOs): > 3.6 min

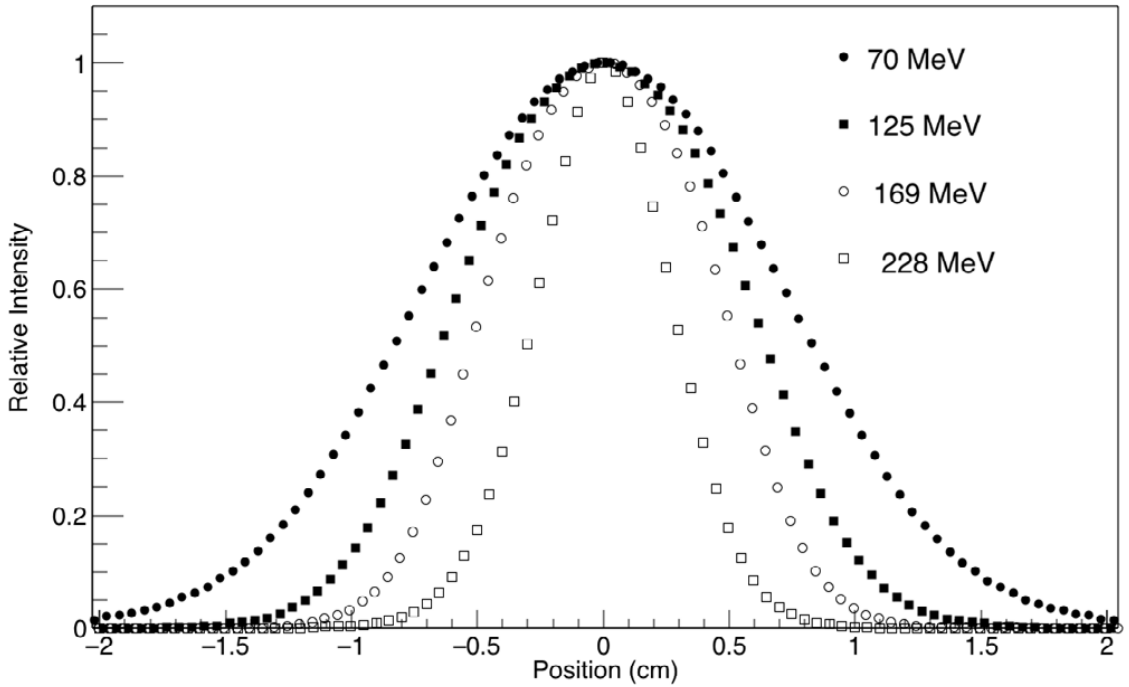
BRAM: $\sigma_{\mathrm{SEU}} = (1.78 \pm 0.23) \cdot 10^{-15} \frac{\mathrm{cm}^2}{\mathrm{bit}}$

MTBF (5.1 Mb) in the dRICH system (1248 RDOs): 2.1 min

SEU cross sections and MTBFs (33 Mb) in the dRICH system (1248 RDOs) for CRAM :

	$\sigma_{\mathrm{SEU}} \left(10^{-16} \frac{\mathrm{cm}^2}{\mathrm{bit}}\right)$	MTBF (min)
COR	(1.96 ± 0.25)	**2.9**
UNCOR	$(3.09 \pm 0.94) \cdot 10^{-1}$	**18**
TOTAL	(2.30 ± 0.28)	**2.5**

Devices and proton beam



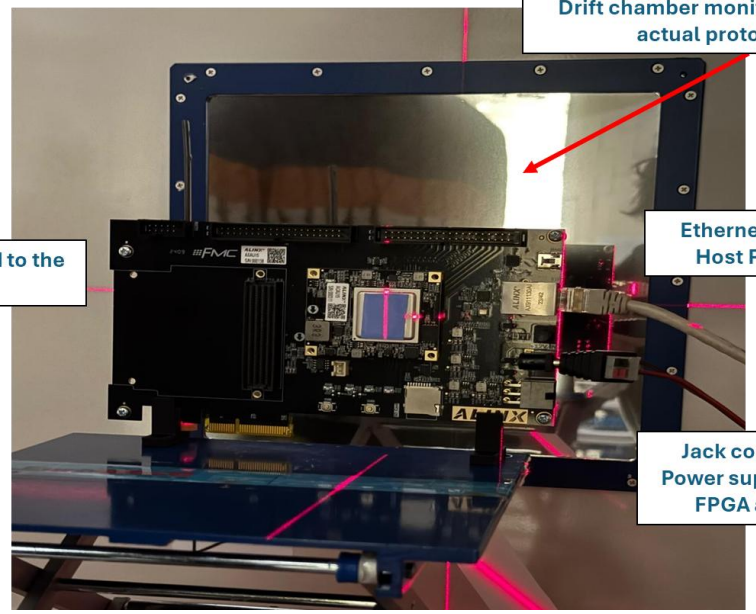
Ref:
https://www.sciencedirect.com/science/article/pii/S0168900217306654

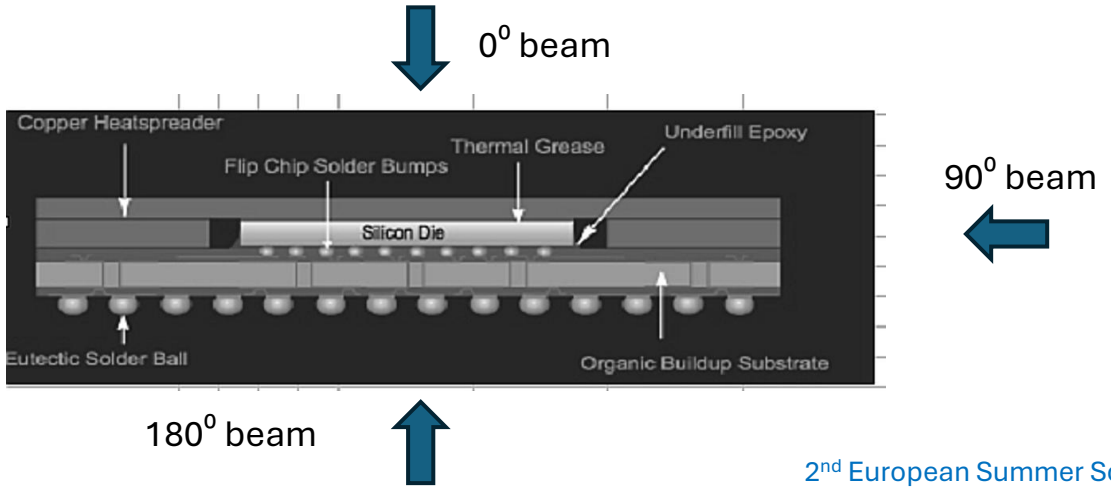
DUT	Area (cm^2)
ATtiny817	0.16
Si5326	0.36
AU15P Die	~1.1

E (MeV)	σ_x (mm)	σ_y (mm)	Asymmetry (%)
70.2	6.93	6.91	0.1
73.9	6.63	6.74	0.8
82.7	6.28	6.41	1.0
90.8	6.04	6.15	0.9
100.0	5.63	5.73	0.8

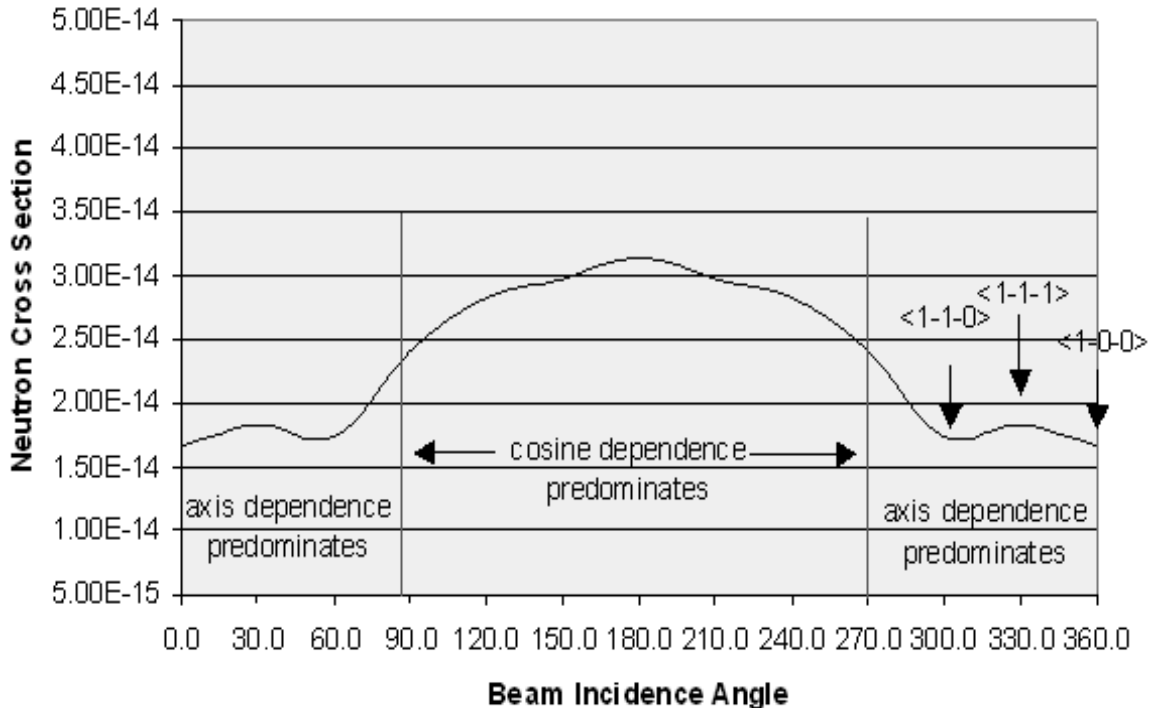
Energy [MeV]	Range [g/cm^2]	FWHM [mm]	Intensity [p/s]
70	4.1	16.2	3.83E+06
74	4.5	15.9	-
83	5.5	15.2	7.50E+06
91	6.5	14.6	9.94E+06
100	7.72	13.7	1.19E+07

Flip-Chip package effect

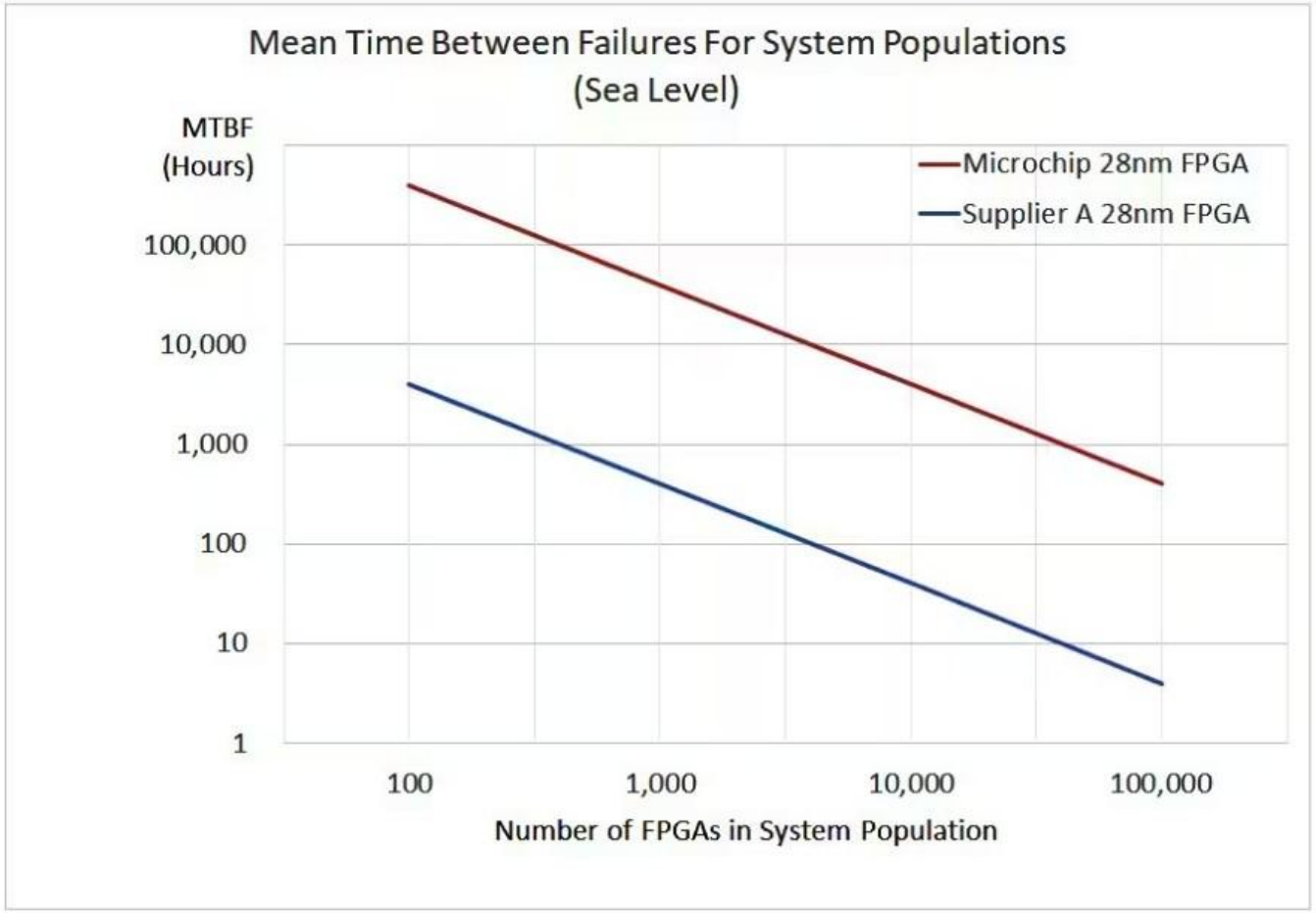




Is the ~**2 factor** for the BRAM SEU cross section **due to the effect of the FPGA package**? Such an effect was shown for the CRAM bits of a Virtex-II FPGA (**ref**: https://www.researchgate.net/publication/3430143).



Configuration memory MTBF for Microchip FPGAs

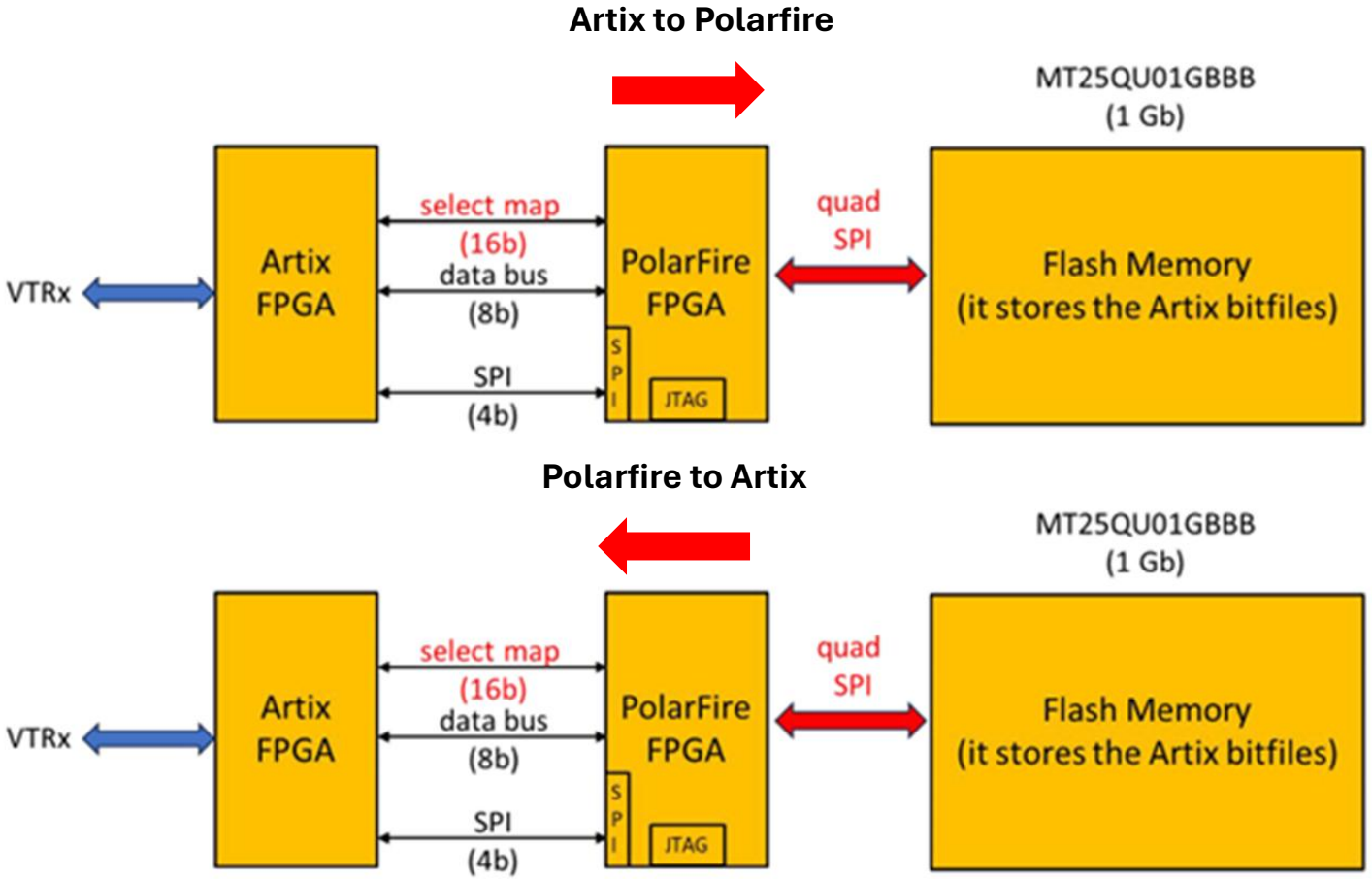


Ref: https://www.microchip.com/en-us/products/fpgas-and-plds/reliability#seus

In this case the **failure** is not the occurrence of a SEU, but it is the **real failure of the FPGA DAQ system**.

AU15P scrubbing

The RDO provides a **FLASH memory that stores the bitfile configuration** of the AU15P FPGA. This device is connected via **SPI protocol signals** to the **MPF050T FPGA**, which performs **AU15P FPGA scrubbing through the 16-bit select_map bus:**

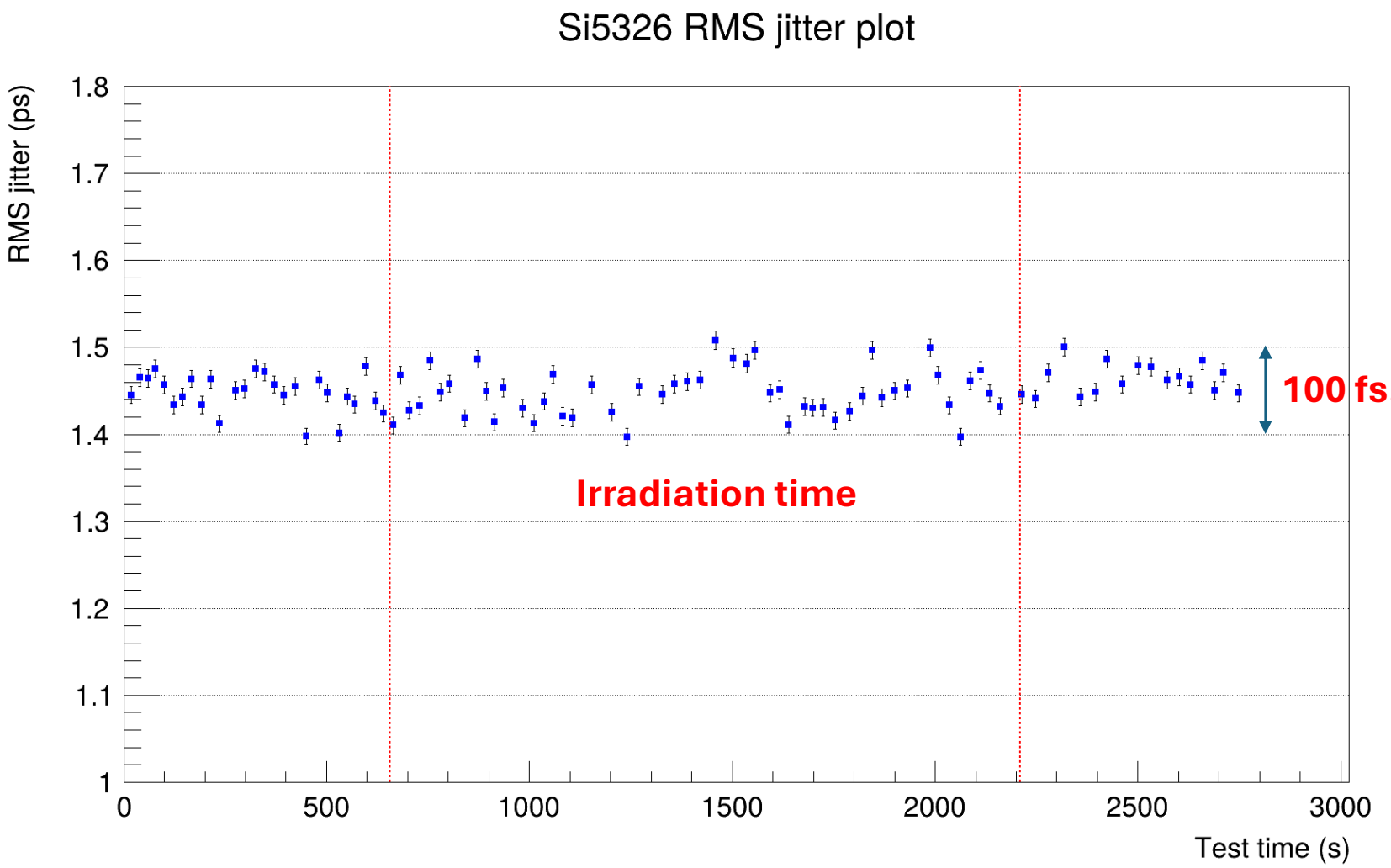


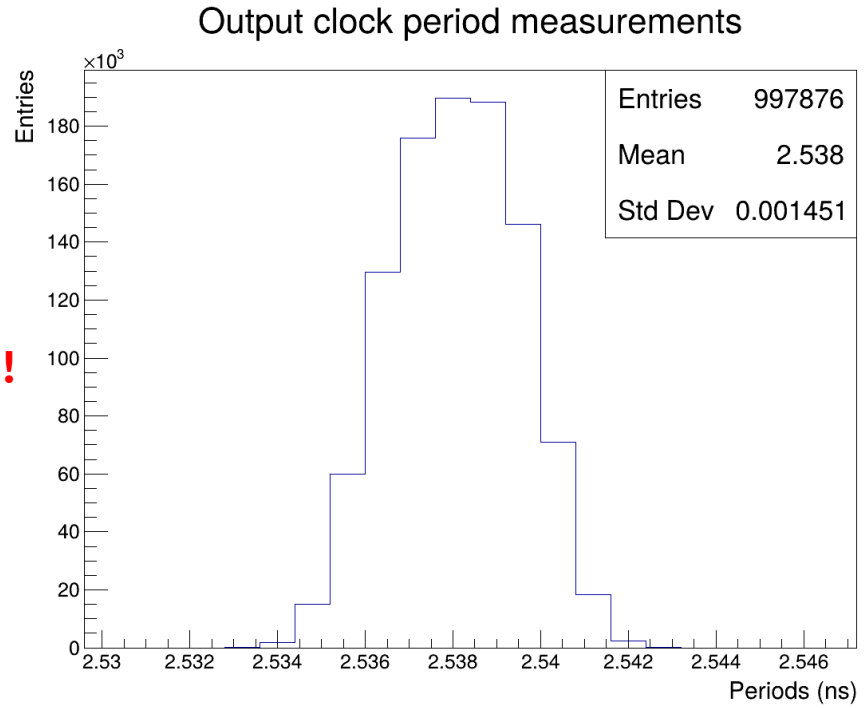
The **MPF050T checks continuously** the AU15P CRAM through the **select_map bus**.

It **compares each address memory** to the one stored in the **FLASH memory (SPI).**

If an **upset is found**, the **MPF050T** will **write the flipped bit via the select_map bus.**

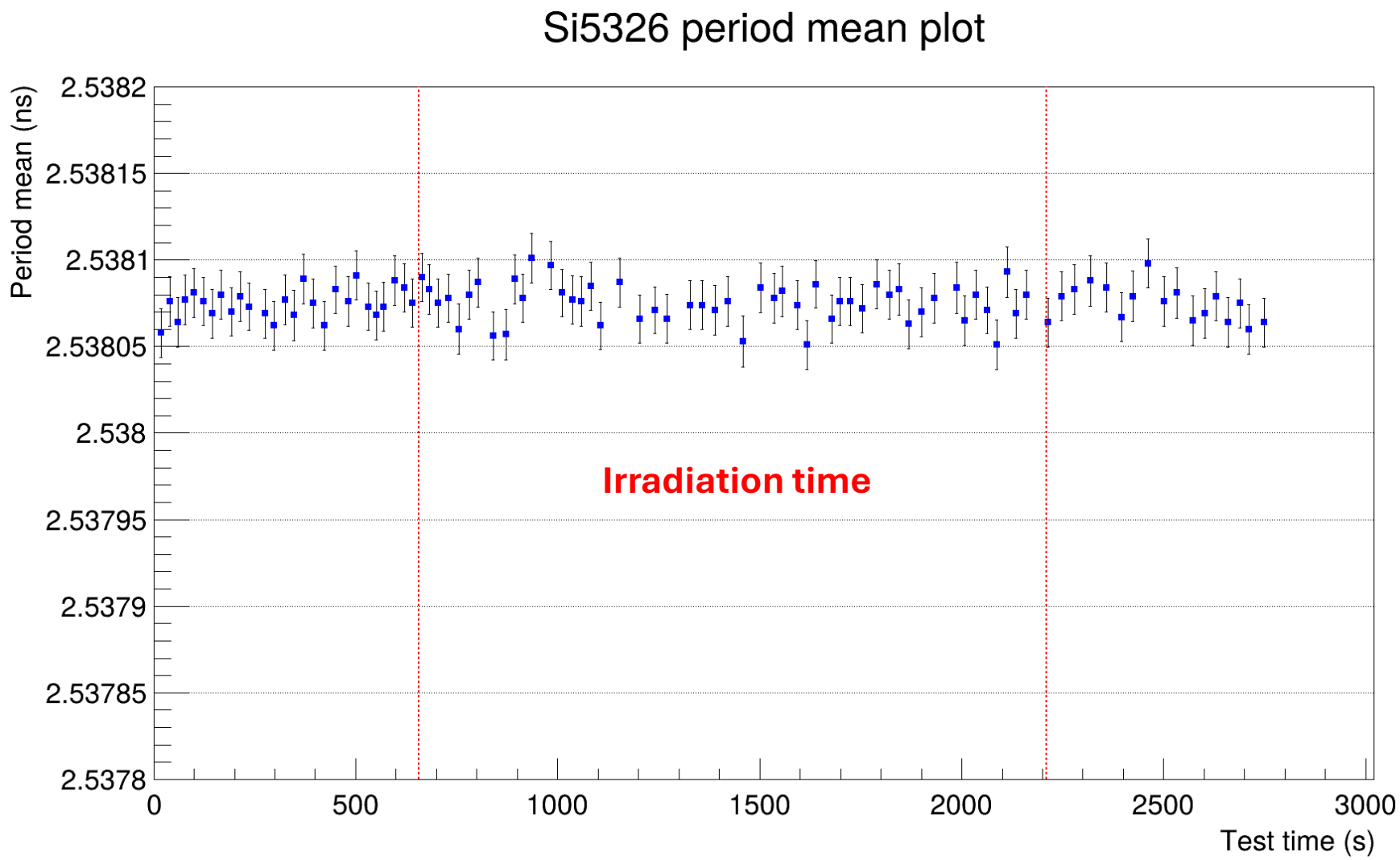
Jitter and period of the output clock



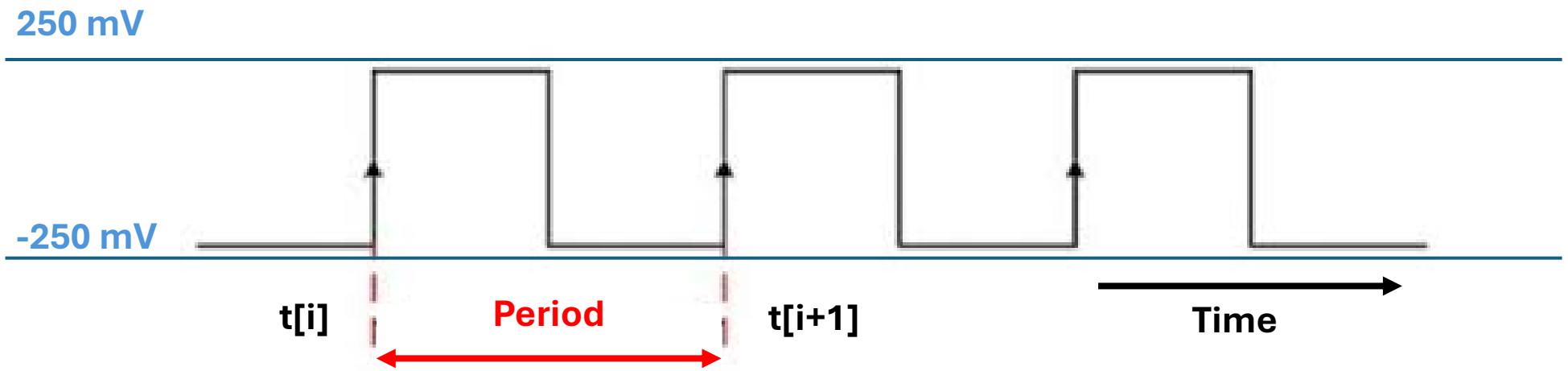


$$f_{ALCOR} = f_{EIC} \cdot 4 = 394\ MHz$$
$$(T = 2.538\ ns)$$

Period mean plot



Period jitter measurement



The **period jitter measurement** was performed as follows:

1. The **0.0 mV transition point** at **each rising edge** was estimated.
2. The period was measured as **t[i+1] – t[i].**
3. **Steps 1. and 2. were repeated after a random number of clock cycles.**

A dataset of **~10^4 periods** was collected:

- The dataset RMS is the **RMS jitter.**
- The dataset mean is the **mean period.**